

Analytical Computation of the Area of Pinched Hysteresis Loops of Ideal Mem-Elements

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Abstract. *The memory elements, memristor being the best known of them, driven by a periodical waveform exhibit the well-known pinched hysteresis loops. The hysteresis is caused by a memory effect which results in a nonzero area closed within the loop. This paper presents an analytical formula for the loop area. This formula is then applied to memory elements whose parameter-vs.-state maps are modeled in the polynomial form. The TiO₂ memristor, a special subset of the above elements, is analyzed as a demonstration example.*

Keywords

Memory element, memristor, pinched hysteresis loop.

1. Introduction

The memory elements, namely memristors, memcapacitors and meminductors [1], driven by periodical waveforms, exhibit the well-known pinched hysteresis loops (PHLs). These loops can be observed in the current-voltage (i - v) coordinates for the memristor, in the charge-voltage (q - v) coordinates for the memcapacitor, and in the flux-current (i - ϕ) coordinates for the meminductor. Since the areas bordered by the loops are specific measures of the memory effect of a device, their evaluation was proposed in several papers [2], [3]. However, the analysis given there is limited to ideal memristors. Note that ideal memristors are defined axiomatically in [4] via unambiguous the charge-flux constitutive relation (CR), which is a generic memristor characteristic, not depending on the way the memristor interacts with other elements in the application network. We should discriminate such memristors from more general memristive systems [5], which can exhibit more complex behavior, violating the basic fingerprints of “ideal” memristors. Analogously, the memcapacitors are defined by their unambiguous TIQ-flux constitutive relations, where TIQ is the abbreviation for time-domain integral of charge [6], [7], also denoted by the

symbol ρ [8]. Such memcapacitors form a subset of more general memcapacitive systems [9]. The meminductors are characterized by their charge-TIF CRs, where TIF, also denoted by the symbol σ [8], means time-domain integral of flux [10]. Meminductors are idealized versions of more general meminductive systems [9].

It is shown in [11] that the CR and the so-called *parameter-vs.-state map* (PSM) are equivalent memristor characteristics. The couples [parameter, state] are [memristance, charge] for the current-controlled memristor, and [memductance, flux] for the voltage-controlled memristor. As shown below, this concept can also be easily extended to other mem-elements. Then the PSM can serve as a universal characteristic for computing the areas of PHLs of memristors, memcapacitors, and meminductors.

In spite of the fact that the areas bordered by pinched hysteresis loops are of various natures, depending on the type of the mem-system, three following reasons for their computation do not depend on their physical interpretation [12]: 1. The area is a specific measure of the memory effect of a system, and its evaluation is useful. 2. Via comparison of the lobe areas, located in the first and third quadrants, such cases can be identified when the systems are not ideal memory elements (then these areas are not equal). 3. If the area does not tend to zero when the frequency of the excitation increases ad infinitum, then we do not have dealings with mem-system [11].

This paper deals with analytical computation of the areas of PHLs of memristors, memcapacitors, and meminductors in the sense of ideal memory elements. That is why the results presented below cannot be generally applied to all memristive, memcapacitive and meminductive systems. The methodology of computing the area of memristor PHL from [3] is utilized. It is extended to all three types of mem-elements, focusing on the cases when the PSM of the element can be approximated by a polynomial. However, the starting procedure of the area computation enables working with arbitrary possible modeling of the PSM [3]. Finally, an example of the computation of the PHL area of the well-known TiO₂ memristor is given.

2. Characteristics of Memory Elements for Computing the PHL Areas

As summarized in [13], the memristors, memcapacitors and meminductors can be described by the uniform equations:

$$y(t) = g(x)u(t), \quad \frac{d}{dt}x(t) = u. \quad (1)$$

Here the variable y represents the element response to the excitation u , and x is the state variable. Tab. 1 summarizes these variables for the voltage-controlled and current-controlled memristors (VCMR and CCMR), voltage-controlled and charge-controlled memcapacitors (VCMC and QCMC), and current-controlled and flux-controlled meminductors (CCML and FCML). The constitutive relation of each element is a single-valued dependence of y_I variable on the state variable, where y_I represents the time-domain integral of the output variable. The element parameters in the PSM function in the last column of Tab. 1 are the memductance G_M , memristance R_M , memcapacitance C_M , inverse memcapacitance D_M , meminductance L_M , and inverse meminductance Λ_M .

element	output y	input u	state x	CR $y(x)$	PSM $g(x)$
VCMR	i	v	φ	$q(\varphi)$	$G_M(\varphi)$
CCMR	v	i	q	$\varphi(q)$	$R_M(q)$
VCMC	q	v	φ	$\rho(\varphi)$	$C_M(\varphi)$
QCMC	v	q	$\rho = TIQ$	$\varphi(\rho)$	$D_M(\rho)$
CCML	φ	i	q	$\sigma(q)$	$L_M(q)$
FCML	i	φ	$\sigma = TIF$	$q(\sigma)$	$\Lambda_M(\sigma)$

Tab. 1. Specification of the variables in (1) for memristors (MR), memcapacitors (MC), and meminductors (ML).

The $g(x)$ function, describing the parameter-vs.-state map, together with the waveform of the input signal $u(t)$, is necessary for computing the area of the PHL described below. The procedure is universal for an arbitrary type of the memory element from Tab. 1.

3. Area Computation from Parameter-vs.-State Map

Consider that the mem-element defined by (1) is driven by a signal

$$u(t) = U_{\max} \sin(\omega t) \quad (2)$$

where U_{\max} , $\omega = 2\pi/T$, and T are the amplitude, angular frequency, and repeating period, respectively. The hysteresis loop of a memristor driven in this way is formed by a closed odd-symmetrical curve Γ in the y - u plane [13], which can be divided into two loops Γ_1 and Γ'_1 as illustrated in Fig. 1.

It follows from the odd symmetry of the pinched hysteresis loop of the mem-element [13] that the areas S_1 and S_2 of the loops are identical but their signs are different. Note that the sign belonging to the area is positive (negative) if the curve surrounding the area is in the clockwise (counter-clockwise) direction. It can be written for the area S_1

$$\begin{aligned} S_1 &= \oint_{\Gamma_1} y du = \oint_{\Gamma_1} g(x) u du = \int_0^{T/2} g(x(t)) u(t) \frac{du}{dt} dt = \\ &= \frac{1}{2} \int_0^{T/2} g(x(t)) \frac{d(u^2)}{dt} dt \end{aligned} \quad (3)$$

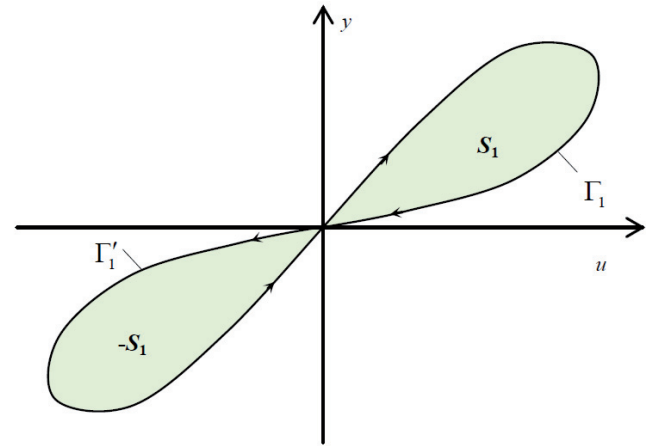


Fig. 1. An example of pinched hysteresis loop of mem-element.

where x is derived via the second equation (1) as follows:

$$x(t) = x_0 + X(1 - \cos(\omega t)). \quad (4)$$

Here x_0 is the state at time $t = 0$, and $X = U_{\max}/\omega \Gamma_1$ is the change of the state variable within one quarter of the repeating period, caused by the input signal. Via *integration by parts*, the rightmost integral in (3) can be modified to the form

$$S_1 = \frac{1}{2} [g(x(t)) u^2]_0^{T/2} - \frac{1}{2} \int_0^{T/2} \frac{d}{dt} [g(x(t))] u^2 dt. \quad (5)$$

Since $u(t)$ is zero at the beginning and also at the end of the half-period, the first right-side term of (5) is zero. A simple arrangement yields the final formula for the loop area

$$S_1 = -\frac{1}{2} \int_0^{T/2} \frac{dg(x)}{dx} u^3 dt. \quad (6)$$

Note that (6) represents a compact formula for computing the area of the pinched hysteresis loop of the mem-element from its universal characteristic (PSM) and from the waveform of the exciting current. Equation (6) holds on the assumption that the function $g(x)$ is differentiable. Formula (6) can also be used if the function $g(x)$ exhibits step discontinuity points. A simple modification for this case is shown in [3].

4. A Case of Mem-Elements with PSM in the Polynomial Form

Consider a mem-element with the PSM in the polynomial form

$$g(x) = g(x_0) + \sum_{i=1}^{\infty} a_i (x - x_0)^i \quad (7)$$

where a_i , $i = 1, 2, \dots$ are real coefficients. Note that the well-known model of TiO_2 memristor with linear dopant drift is a subset of this case defined as [14]

$$a_1 = -(R_{OFF} - R_{ON})k, a_i = 0 \text{ for } i > 1, \quad (8)$$

where R_{OFF} and R_{ON} are the maximum and minimum resistances of the memristor, and k is a material constant [14], [15]. The model is true if the memristor is excited by current, thus $u(t) = i(t)$.

Substituting (7) and (2) into (6) and re-arranging yield the loop area

$$S_1 = -\frac{U_{\max}^3}{2\omega} \sum_{i=1}^{\infty} i a_i X^{i-1} \int_0^{\pi} \sin^3 \alpha (1 - \cos \alpha)^{i-1} d\alpha \cdot \quad (9)$$

Considering the equalities

$$\int_0^{\pi} \sin^3 \alpha (1 - \cos \alpha)^{i-1} d\alpha = \frac{2^{i+2}}{(i+1)(i+2)} \quad (10)$$

and $X = U_{\max}/\omega$, the universal formula of the loop area of the mem-element with the characteristic $g(x)$ of type (7), driven by signal (2), is as follows:

$$S_1 = -\sum_{i=1}^{\infty} a_i \frac{i}{(i+1)(i+2)} 2^{i+1} \frac{U_{\max}^{i+2}}{\omega^i}. \quad (11)$$

5. Experimental Verification

In order to verify the above method, formula (11) has been used for evaluating the area of the PHL of TiO_2 memristor (8), which is driven by a sinusoidal current

$$i(t) = I_{\max} \sin(\omega t). \quad (12)$$

Considering (8), equation (11) is as follows:

$$S_1 = \frac{2}{3} (R_{OFF} - R_{ON}) k \frac{I_{\max}^3}{\omega}, \quad (13)$$

i.e. the area is directly proportional to the third power of the amplitude of the driving current and this area diminishes hyperbolically with increasing frequency. This result is in conformity with [3]. Note that the loop area does not depend on the initial charge q_0 or on the initial value of the memristance at the beginning of memristor excitation. The reason consists in the linear dependence of the memristance on the charge. Then the polynomial approximation (7) does not depend on the central point x_0 of the expansion of $g(x)$ function.

The above results, obtained analytically, were verified via SPICE simulations. The TiO_2 memristor with linear dopant drift was modeled as in [15] but with rectangular window function. The simulation results are shown in Fig. 2, together with the simulation conditions specified in the figure caption. The areas of the 1st quadrant loops were computed via a special measuring function in PROBE [12] and compared to the exact result from (13). For all the loops in Fig. 2, the measuring functions provided the same area value $1.0498 \mu\text{VA}$, which slightly differs from the theoretical value $1.0504 \mu\text{VA}$ due to numerical errors.

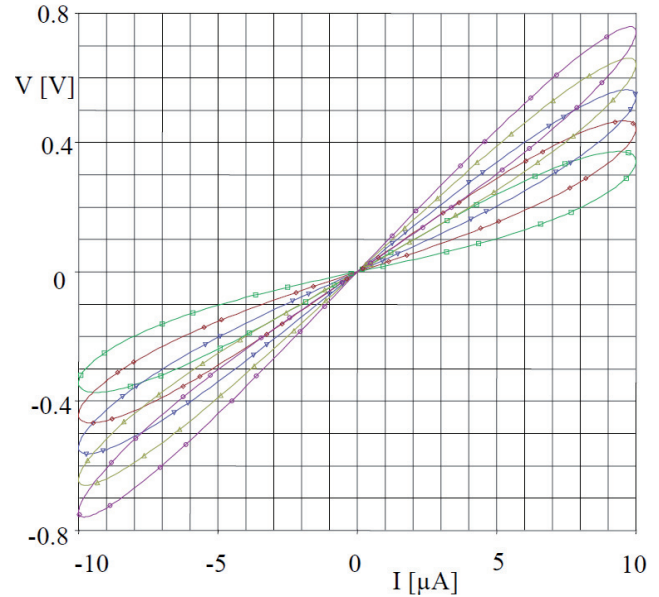


Fig. 2. The loop area of the TiO_2 memristor does not depend on the initial memristance. Simulation conditions: $I_{\max} = 10 \mu\text{A}$, $f = 1 \text{ Hz}$, $R_{ON} = 1 \text{ k}\Omega$, $R_{OFF} = 100 \text{ k}\Omega$, $k = 10^5 \text{ C}^{-1}$. Initial value of the memristance is stepped from $50 \text{ k}\Omega$ (green loop) to $90 \text{ k}\Omega$ (magenta loop) with a linear step of $10 \text{ k}\Omega$.

6. Conclusion

Analytical formula (11) for computing the area of the hysteresis loop, derived from general equation (6), is useful for those memory elements whose parameter-vs.-state map can be approximated via polynomial functions. This assumption is true, for example, for the well-known model [14] of the TiO_2 memristor. Based on the specifications in Tab. 1, the procedure described in the paper can easily be applied to arbitrary memory elements listed in this table.

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References

- [1] Di VENTRA, M., PERSHIN, Y. V., CHUA, L. O. Circuit elements with memory: memristors, memcapacitors, and meminductors. *Proceedings of the IEEE*, 2009, vol. 97, no. 10, p. 1717 – 1724.
- [2] RADWAN, A. G., ZIDAN, M. A., SALAMA, K. N. On the mathematical modeling of memristors. In *Proc. 22nd Int. Conf. on Microelectronics (ICM 2010)*. Cairo (Egypt), 2010, p. 284 – 287.
- [3] BIOLEK, Z., BIOLEK, D., BIOLKOVÁ, V. Computation of the area of memristor pinched hysteresis loop. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2012, no. 9, p. 607 – 611.
- [4] CHUA, L. O. Memristor—the missing circuit element. *IEEE Transactions on Circuit Theory*, 1971, vol. CT-18, no. 5, p. 507 – 519.
- [5] CHUA, L. O., KANG, S. M. Memristive devices and systems. *Proc. of the IEEE*, 1976, vol. 64, no. 2, p. 209 – 223.
- [6] BIOLEK, D., BIOLEK, Z., BIOLKOVÁ, V. Behavioral modeling of memcapacitor. *Radioengineering*, 2011, vol. 20, no. 1, p. 228 to 233.
- [7] BIOLEK, D., BIOLKOVÁ, V., KOLKA, Z. Mutators simulating memcapacitors and meminductors. In *Proc. of the 11th biennial IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2010)*. Kuala Lumpur (Malaysia), 2010, p. 800 – 803.
- [8] BAATAR, C., POROD, W., ROSKA, T. *Cellular Nanoscale Sensory Wave Computing*. Springer, 2011.
- [9] PERSHIN, Y. V., Di VENTRA, M. Memory effects in complex materials and nanoscale systems. *Advances in Physics*, 2011, vol. 60, p. 145 – 227.
- [10] BIOLEK, D., BIOLEK, Z., BIOLKOVÁ, V. PSPICE modeling of meminductor. *Analog Integrated Circuits and Signal Processing*, 2011, vol. 66, no. 1, p. 129 – 137.
- [11] CHUA, L. O. Resistance switching memories are memristors. *Applied Physics A*, 2011, no. 102, p. 765 – 783.
- [12] BIOLEK, D., BIOLEK, Z., BIOLKOVÁ, V., KOLKA, Z. Computing areas of pinched hysteresis loops of mem-systems in OrCAD PSPICE. *Applied Mechanics and Materials*, 2013, vols. 278-280, p. 1081-1090.
- [13] BIOLEK, D., BIOLEK, Z., BIOLKOVÁ, V. Pinched hysteretic loops of ideal memristors, memcapacitors and meminductors must be 'self-crossing'. *Electronics Letters*, 2011, vol. 47, no. 25, p. 1385 – 1387.
- [14] STRUKOV, D. B., SNIDER, G. S., STEWART, D. R., WILLIAMS, R. S. The missing memristor found. *Nature*, 2008, vol. 453, p. 80 – 83.
- [15] BIOLEK, Z., BIOLEK, D., BIOLKOVÁ, V. SPICE model of memristor with nonlinear dopant drift. *Radioengineering*, 2009, vol. 18, no. 2, p. 210 – 214.

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